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MEMS for Harsh Application Environments

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4.1 Overview

Use of silicon (Si) as a mechanical material has enabled the development of a broad range of solid-state sensors and actuators that are well suited for many aerospace applications. Unfortunately, the high-temperature operating limit for these devices is about 250°C, due in large part to degradation in electrical performance above 250°C, a significant decrease in the elastic modulus above 600°C, and temperature limitations of metal contacts. Therefore, many application areas, such as engine instrumentation, cannot benefit from microelectromechanical systems (MEMS) without expensive and bulky packaging schemes to keep Si-based MEMS devices below their high-temperature limit. Wide band-gap semiconductors offer promise for the development of high-temperature MEMS, because these materials have stable electronic properties at high temperatures. In addition, wide band-gap semiconductors such as silicon carbide (SiC) and diamond have outstanding mechanical properties, excellent chemical inertness, and high radiation resistance, which are attractive properties for aerospace applications.

This chapter provides the reader with an overview of SiC as a semiconductor for MEMS in harsh environments. The focus is on SiC because it is the leading material for high-temperature MEMS. The chapter will open with a presentation of the material properties and microstructure of SiC, followed by sections on thin-film growth, processing techniques, micromachining of SiC, and SiC-on-insulator technologies. The chapter will conclude with a review of SiC-based MEMS devices that are suitable for aerospace applications.

4.2 Material Properties of SiC

4.2.1 Introduction

Semiconductors to be used in high-temperature MEMS should have a wide band gap, high thermal conductivity, and excellent mechanical stability at elevated temperatures. Based on these properties, the most attractive materials are diamond and SiC. Prototype MEMS devices have been fabricated from both materials.[1,2] However, SiC has a number of distinct advantages over diamond, which has made SiC the leading material for MEMS in harsh environments. Economic issues require MEMS materials to be compatible with batch fabrication, preferably, batch fabrication processes used in the Si integrated circuit (IC) industry, which necessitates the use of large-area substrates. Single and polycrystalline SiC films can be grown on large-area Si wafers; whereas diamond can only be deposited in polycrystalline form on Si substrates. Another advantage of SiC is that numerous Si-compatible plasma etch processes have been developed to pattern SiC films; whereas diamond films are not readily patterned. Despite these advantages of SiC, diamond is still an attractive high-temperature material for MEMS applications. Details concerning film growth, patterning, device fabrication, and performance can be found in the literature.[3–5] The remainder of this chapter will concentrate on the development and implementation of SiC as a MEMS material for harsh environments.

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4.2.2 Properties of SiC

SiC has long been recognized as a semiconductor with outstanding physical and chemical characteristics. Compared to Si, SiC exhibits a larger band gap, a higher breakdown field, a higher thermal conductivity, and a higher saturation velocity. These properties make SiC a very attractive material for the fabrication of high-temperature, high-power, and high-frequency electronic devices. Moreover, a high elastic modulus and high hardness make SiC an excellent material for the mechanical components in high-temperature microsensors and microactuators. High-temperature microsensors and microactuators can be used for pressure sensing, temperature sensing, and chemical sensing in gas turbine engines. SiC also has a higher chemical inertness and radiation resistance than Si, which expands its potential as a material for sensors and actuators in satellite and other space systems.

4.2.3 Crystal Structure

Any discussion of SiC as a material for microdevices requires an understanding of the crystalline structure of SiC. SiC exhibits a one-dimensional polymorphism called polytypism. All polytypes of SiC have a common planar arrangement of Si and C atoms, but each polytype is distinguished by a unique stacking sequence of the identical planes. Disorder in the stacking periodicity of the similar planes results in a material that has numerous crystal structures (polytypes), all with the same atomic composition. The magnitude of the disorder is such that over 250 SiC polytypes have been identified to date.[6] Despite the large number of polytypes, only three crystalline symmetries exist: cubic, hexagonal, and rhombohedral. Historically, the cubic phase of SiC has been referred to as ß-SiC, and the hexagonal and rhombohedral phases have been called α-SiC. Recently, a more descriptive nomenclature that identifies both the crystalline symmetry and stacking periodicity has been adopted. Using this system, cubic SiC is called 3C-SiC, which is the only cubic polytype known to exist. The most common α-SiC polytypes have hexagonal symmetries and are called 6H-SiC, 4H-SiC, and 2H-SiC.

4.2.4 Physical Characteristics

Even though polytypes have the same atomic composition, the electrical properties of each polytype are different. For instance, the band gap for SiC ranges from 2.3 eV for 3C-SiC to 3.4 eV for 2H-SiC. Due, in part, to its cubic crystalline symmetry, 3C-SiC has the highest electron mobility (1000 $cm^2/V \cdot s$) and saturation drift velocity ($10^7 cm/s$).

SiC has long been noted for its hardness, wear resistance, and chemical inertness. SiC has a Mohs hardness of 9, which compares favorably with values for other hard materials, such as diamond (10) and topaz (8). In terms of wear resistance, SiC has a value of 9.15, as compared with 10 for diamond and 9 for Al_2O_3. SiC can be etched by alkaline hydroxide bases (i.e., potassium hydroxide [KOH]), but only at very high temperatures (~600°C), and is not etched by acids. SiC does not melt, but sublimes above 1800°C. The surface of SiC can be passivated by the formation of a thin thermal SiO_2 layer, but the oxidation rate is very low when compared with that of Si. A summary that compares the important semiconductor properties of 3C-SiC and 6H-SiC with those of other noted semiconductors is presented in Table 4.1.

4.3 Thin Film Growth

4.3.1 Homoepitaxy of 6H-SiC

A major impediment to the commercialization of SiC as a high-temperature semiconductor is the availability of large-area, high-quality, defect-free SiC substrates suitable for epitaxial growth. Although 3C-SiC has the least complex crystal structure of all the SiC polytypes, bulk crystal growth of high-quality 3C-SiC is very difficult, and no wafer-grade substrates have been

Table 4.1. Important Properties of High-Temperature Semiconductors

Property	3C-SiC (6H-SiC)	GaAs	Si	Diamond
Melting point (°C)	> 1800[a]	1238	1415	1400[b]
Thermal conductivity (W/cm°C)	5	0.5	1.5	20
Coeff. thermal expan. ($°C^{-1}\times10^{-6}$)	4.2	6.86	2.6	1.0
Young's modulus (GPa)	448	75	190	1035
Physical stability	Excellent	Fair	Good	Fair
Bandgap (eV)	2.2 (2.9)	1.424	1.12	5.5
Electron mobility ($cm^2/V\cdot s$)	1000 (600)	8500	1500	2200
Hole mobility ($cm^2/V\cdot s$)	40	400	600	1600
Breakdown voltage (10^6V/cm)	4	0.4	0.3	10
Dielectric constant	9.72	13.1	11.9	5.5

[a] Sublimation temperature.
[b] Phase change temperature.

fabricated. Several companies have developed successful processes to grow high-quality bulk 6H-SiC crystals, and 2-in.-diam electronic-grade wafers are commercially available. Unfortunately, these wafers are relatively expensive, which limits their use to low-volume, high-cost applications.

Development of SiC has focused on 6H-SiC for high-temperature, high-power, and high-frequency microelectronics, and a detailed review has been recently published.[7] For high-temperature electronic devices, high quality n- and p-doped single-crystal SiC films are required. A common method for growing homoepitaxial 6H-SiC films on 6H-SiC substrates uses atmospheric-pressure chemical vapor deposition (APCVD) with Si- and C-containing gases and high substrate temperatures (1500°C–1700°C). Commonly used precursor gases are silane (SiH_4) and propane (C_3H_8), with H_2 as a carrier gas. Typical dopant gases are trimethyl-aluminum [$Al(CH_3)_3$] and diborane (B_2H_6) for p-type films, and N_2, ammonia (NH_3), and phosphene (PH_3) for n-type films.

4.3.2 Heteroepitaxy of 3C-SiC on Si

Unlike the other polytypes, single-crystal 3C-SiC, hereafter simply called 3C-SiC, can be heteroepitaxially grown on Si substrates by both APCVD and low-pressure chemical vapor deposition (LPCVD). The most common APCVD process uses H_2 as the carrier gas, SiH_4 as the Si source gas, and C_3H_8 as the C source gas.[8] Other processes use dichlorosilane as a Si source, and acetylene as a C source.[9] Single C- and Si-containing sources, such as methyltrichlorosilane (CH_3SiCl_3) and methylsilane (CH_3SiH_3), have also been used to grow 3C-SiC by LPCVD.[10,11] Heteroepitaxy is possible because 3C-SiC and Si have similar cubic crystal structures: 3C-SiC has a zinc-blend structure with a lattice constant of 0.436 nm, while Si has a diamond structure with a lattice constant of 0.543 nm, resulting in a lattice mismatch of approximately 20%. A process called carbonization is often used to initiate heteroepitaxial growth by forming a thin 3C-SiC film directly from the Si substrate. Carbonization converts the near surface region of the Si substrate to 3C-SiC by exposing a heated substrate to a carbon-containing gas. Carbonization temperatures range from 1250°C to 1360°C, depending on the process. The carbon-containing gas dissociates

into hydrocarbon reactants, which react with Si on the wafer surface, forming a thin, heteroepitaxial 3C-SiC film. Because SiC films are excellent diffusion barriers, the carbonization process is self-limiting. Film growth is continued by introducing a Si-containing gas to the flow, which initiates homoepitaxial growth of 3C-SiC on the heteroepitaxial 3C-SiC carbonization layer. 3C-SiC films as thick as 40 μm have been grown on small Si substrates.[12] Moreover, 3C-SiC films have been grown on large-area Si wafers (4-in.-diam),[13] enabling the batch fabrication of 3C-SiC MEMS devices.

Despite the obvious advantage of growing 3C-SiC films on inexpensive, large-area Si wafers, heteroepitaxial 3C-SiC films suffer from a large density of crystalline defects. The large defect density results, in part, from the 20% lattice mismatch, but also from an 8% difference in thermal expansion coefficients between 3C-SiC and Si. The defect density is highest at the SiC/Si interface and decreases with increasing film thickness. Unfortunately, the defect density in heteroepitaxial 3C-SiC films is not low enough to make the performance of 3C-SiC electronics comparable with 6H-SiC and Si devices. However, the crystal quality of 3C-SiC may be good enough for high-temperature microsensor applications.

Another troubling problem associated with 3C-SiC heteroepitaxy on Si substrates is the formation of voids at the SiC/Si interface. These voids are sealed microcavities and are common to samples grown by most APCVD and LPCVD processes. The void density can be quite high, with values as high as 10^5 voids/cm^2 reported in the literature.[12] Voids compromise the contact between the 3C-SiC film and the Si substrate, and may contribute to the large defect density in 3C-SiC films. The mechanism for void formation is not clear. However, it has been suggested that voids result from Si out-diffusion from uncarbonized regions of the Si surface during the carbonization process.[14] Void formation also appears to be dependent on the temperature ramp-up rate during the carbonization step. Typically, high ramp-up rates of about 50°C/s are used. Void densities as low as 2 voids/cm^2 have been achieved when low ramp-up rates (~3°C/s) are used.[13] Others[15,16] have since developed growth processes with similar results.

As mentioned previously, the main advantage of 3C-SiC from a MEMS perspective is that 3C-SiC can be heteroepitaxially grown on Si substrates, which enables 3C-SiC growth on inexpensive, large-area wafers. Using an APCVD process, uniform heteroepitaxy of 3C-SiC across 4-in. Si wafers has been demonstrated.[13] Additionally, a LPCVD reactor has been used to grow 3C-SiC films on multiple 4- and 6-in. Si wafers.[17]

4.3.3 Polycrystalline SiC

For many MEMS applications, polycrystalline SiC can be used. Unlike 3C-SiC and 6H-SiC, polycrystalline 3C-SiC, hereafter called poly-SiC, can be deposited on a wide variety of substrate types, including suitable sacrificial layers such as SiO_2. Poly-SiC has been deposited by plasma-enhanced chemical vapor deposition (PECVD), sputtering, and electron beam evaporation at substrate temperatures ranging from 200°C to 1000°C.[18–20] These films are either amorphous, as in the case with low-temperature PECVD, or polycrystalline, with a texture dependent on deposition temperature. APCVD and LPCVD processes have been used to deposit poly-SiC on Si substrates, resulting in films with microstructures much like the aforementioned films.[21,22]

Traditionally, APCVD has been used to grow 3C-SiC films on Si substrates and 6H-SiC films on 6H-SiC substrates. Recently, however, APCVD has been used to deposit SiC films on polysilicon substrates.[23] Polysilicon was chosen because of its potential as a sacrificial layer in a SiC-based surface micromachining process. As mentioned previously, SiC etching in KOH is not practical, except at temperatures above 600°C; whereas Si is readily etched in KOH at temperatures below 70°C. Thus, a 2- to 3-μm-thick polysilicon layer deposited on a thermally oxidized

Si wafer provides an excellent substrate for a SiC surface micromachining process that uses KOH as a release agent. In this study, poly-SiC films were grown on polysilicon using the traditional 3C-SiC APCVD growth process. Two types of polysilicon films were used as substrates: (1) as-deposited polysilicon, and (2) annealed polysilicon. The annealing time was such that the as-deposited polysilicon, which is highly oriented in the [110] direction, was completely recrystallized during the process. The annealed polysilicon is a mixture of (220) and (111) crystallites. X-ray diffraction (XRD) and transmission electron microscopy (TEM) were used to characterize the films. Polycrystalline SiC grown on as-deposited polysilicon has a texture that closely resembles the as-deposited polysilicon substrate, despite the fact that during the growth process, the underlying polysilicon is fully recrystallized. The recrystallization process does not modify the crystallinity or adversely affect the adhesion of the poly-SiC films. Poly-SiC films grown on fully recrystallized (annealed) polysilicon exhibit a grain-to-grain epitaxial relationship with the substrate. It is well established that for polysilicon films, texture influences such physical properties as oxidation rate, thermal conductivity, elastic modulus, and film stress.[24–26] The same may also be true for poly-SiC. This process makes possible the ability to grow highly textured poly-SiC by controlling the substrate texture.

The most straightforward surface micromachining process uses an insulating film, like SiO_2, as the sacrificial substrate material. Poly-SiC films have been sputter deposited and reactively evaporated on SiO_2 substrates, but only recently has APCVD been used.[27] No carbonization of the SiO_2 layer was necessary, so a single-step film growth process was used. It was reported that films grown at 1050°C and 1160°C exhibited good adhesion to the SiO_2 substrates, while films deposited at 1280°C delaminated during or shortly after film growth. At lower growth temperatures, the poly-SiC films were randomly oriented, with grain size increasing with increasing temperature. Lower deposition temperatures resulted in the deposition of Si-rich poly-SiC films, although the excess Si concentration was less than 10 at%.

4.3.4 APCVD or LPCVD

APCVD and LPCVD are the two most versatile techniques to deposit SiC for MEMS applications, since APCVD and LPCVD can be readily used to deposit both 3C-SiC and poly-SiC. This capability enables the fabrication of hybrid sensors and actuators that consist of 3C-SiC electronics coupled with poly-SiC mechanical components. LPCVD is noted for producing films with a high degree of thickness uniformity (<5% variation), although the growth rates for 3C-SiC tend to be low (~0.1 μm/h).[22] LPCVD is particularly well suited for batch fabrication, since film growth can be performed in furnace tubes that can accommodate numerous large-area wafers. APCVD films are grown at a much higher rate (1–2 μm/h); however, thickness uniformity on large-area substrates varies by as much as 30%,[13] and only one or two 4-in. wafers can be loaded in each deposition run.

4.4 Processing Techniques

4.4.1 Introduction

As mentioned previously, SiC films can be processed using many of the standard processing tools common to Si IC fabrication. Thermal oxidation, metallization, and plasma etching can be performed in a Si fabrication facility without any major retooling. In terms of materials compatibility, it has been shown that SiC processing does not lead to contamination of Si processing equipment.[28] In fact, poly-SiC is now being used as an alternative to quartz for wafers, wafer boats, susceptors, and other components used in Si furnaces.

4.4.2 Oxidation

Unlike for diamond, stable thermal oxides can be grown on SiC. In fact, standard Si thermal oxidation processes are used to grow thermal oxides on SiC, even though the fundamental oxidation mechanism is different. For example, oxidation of Si is achieved by the direct reaction of Si with O_2 to form SiO_2; whereas SiC reacts with O_2 to form SiO_2 and CO during the SiC oxidation process.[7] Because SiC is more chemically stable than Si and thereby less likely to react with O_2, the time required to form a thermal oxide of equivalent thickness is longer for SiC. For example, a process used to form a 1.5-μm-thick thermal oxide on Si yields only a 900-Å-thick thermal oxide on 3C-SiC. As with Si oxidation, H_2 enhances the oxidation rate of SiC.

Many MEMS applications require thick (>1 μm) oxides that cannot be achieved, with reasonable feasibility, by thermal oxidation of SiC. As an alternative to direct thermal oxidation, SiO_2 layers can be "deposited" on SiC by first depositing a polysilicon film onto the SiC substrate, then converting the entire polysilicon film to SiO_2 by thermal oxidation.[29] This process takes advantage of well-established polysilicon deposition and oxidation techniques. Also, because the oxide is formed by thermal oxidation, it has favorable high-temperature properties. SiO_2 thicknesses of well over 1.5 μm can be achieved by thermal oxidation. An example that uses this technique as part of a wafer-bonding process will be presented later in this chapter.

4.4.3 Metallization

Several comprehensive reviews have recently been published that summarize the research conducted on electrical contacts to SiC.[30,31] In general, the best high-temperature contacts are metals with high melting temperatures, such as Ni and W. These metals can be used to form either ohmic or Schottky contacts to 3C-SiC and 6H-SiC. This section will focus only on metal contacts to 3C-SiC.

The best and most widely used ohmic contact to 3C-SiC is Al. Al is the preferred ohmic contact because it is easily deposited by sputtering and evaporation, it is commonly used in silicon processing, and a wire bonding/packaging technology for Al currently exists. Unfortunately, Al melts at about 600°C, making it unsuitable for high-temperature contacts. Sputter-deposited Ni, W, Mo, and other complementary metal oxide semiconductor (CMOS) compatible refractory metals make ohmic contacts to 3C-SiC after a short high-temperature (i.e., 900°C for Ni) post-deposition anneal. Binary compounds such as $TiSi_2$ and WSi_2, and alloys like Au-Ta, are also ohmic contacts to 3C-SiC.

The best Schottky contact to 3C-SiC is Au. Like Al, Au is easily deposited, and a wire bonding/packaging technology currently exists. Unfortunately, Au is not a Si-compatible metal, so care must be taken when using Au. Although Au has a relatively high melting temperature, it is not a suitable high-temperature contact material, because of electromigration at relatively low temperatures. High-melting point metals like Ti and Ni have shown Schottky behavior on 3C-SiC. Comprehensive tables summarizing the deposition conditions and evaluation data for metal contacts to n- and p-type 3C-SiC are presented in Ref. 30.

4.4.4 Plasma Etching

Selective etching is required to pattern the SiC films into the desired structural components for a MEMS device. For Si-based devices, patterning can be performed by dry (plasma) or wet chemical etching. Although wet chemical etching of SiC is not feasible, plasma etching techniques have been developed.[32–34] These techniques use nearly the same F-based plasma chemistries developed for Si, SiO_2, and Si_3N_4 films. Commonly used fluorinated compounds are CF_4, CHF_3, NF_3, and SF_6. Usually, etching is conducted in reactive ion etching (RIE) mode, meaning that pressures are kept below 200 mtorr and sputtering of the substrate is suppressed. For the most

part, these techniques are effective for device fabrication. However, the etch rates for SiC are relatively low when compared with etch rates for Si under similar conditions.

Most RIE processes for SiC require plasmas consisting of O_2 mixed with a fluorinated compound. Unfortunately, common photoresists are not resistant to these highly oxygenated plasmas and cannot be used to etch micron-thick SiC films. Therefore, other masking materials, such as Al, are used. Al is effective as a masking material, but may be responsible for a phenomenon called micromasking. Micromasking occurs when sputtered material from the chamber or etch mask is deposited in the etch field and forms small masks that shield the underlying etch field from the plasma. If the etching process has a high degree of anisotropy, micromasks will produce undesirable "grasslike" structures in the etch field. Decreasing the anisotropy of the plasma can undercut and eliminate the micromasks, but will also reduce the anisotropy of the etched features. Using graphite electrodes[35] or adding small concentrations of hydrogen to the plasmas reduces the micromasking effect.[36]

Etch selectivity is another key issue facing the SiC MEMS processing. SiC-surface micromachining processes utilize SiO_2 and polysilicon films for sacrificial layers, and SiO_2 films for dielectric isolation. In general, plasma conditions that etch SiC at high rates, etch SiO_2 and polysilicon at even higher rates. Some progress has been made in improving the etch selectivities of SiC to Si and SiO_2. The best reported selectivities for room temperature etching were 2:1 for SiC to Si, and 1:3.6 for SiC to SiO_2.[37] Because these selectivities are nowhere near ideal for micromachining, great care must be taken when etching SiC on Si and SiO_2 substrate materials. Examples of SiC-based MEMS devices that utilized plasma etching during the fabrication process will be presented later in this chapter.

4.5 Micromachining of SiC

4.5.1 Bulk Micromachining

As stated previously, bulk micromachining of SiC is very difficult, because of its outstanding chemical stability. Standard Si bulk micromachining techniques that use KOH or ethylenediamine pyrocatechol (EDP) are not effective in etching SiC. Some success in bulk micromachining of SiC using nonstandard techniques has been demonstrated. For instance, a laser-assisted photoelectrochemical etching (PEC) technique for n-type 3C-SiC has been developed.[38] Subsequently, an n-type 3C-SiC etch process that uses a p-type 3C-SiC etch stop was demonstrated.[39] PEC has since been extended to 6H-SiC and was successfully used in a pressure sensor fabrication process.[40]

For MEMS applications such as pressure sensing, hybrid structures consisting of SiC films on bulk micromachined Si substrates have been investigated. Si bulk micromachining techniques are well suited for fabricating these structures. The resistance of SiC to Si etchants is so high that SiC is an excellent etch stop for Si bulk micromachining. The most basic hybrid structure is a 3C-SiC membrane on a Si substrate. A cross section of the simple fabrication process is shown in Fig. 4.1. A 3C-SiC film of the desired thickness is first grown on a Si substrate. A thermal oxide is then grown on both sides of the sample. The back-side oxide is photolithographically patterned to form a KOH-resistant diaphragm mask, and the front-side oxide is etched off the 3C-SiC surface. The sample is then immersed in a KOH etch bath to etch away the exposed regions of Si to form the SiC diaphragms. The potential of this technique for batch fabrication was demonstrated when approximately 275 2-μm-thick 3C-SiC diaphragms were successfully fabricated on a single 4-in. Si wafer.[41]

Fundamental to the success of SiC-based MEMS is a thorough understanding of the mechanical properties of SiC films. Bulk-micromachined SiC diaphragms have been used extensively as

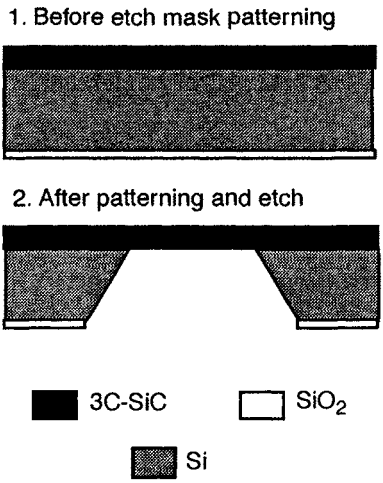

Fig. 4.1. Schematic diagram of the bulk micromachining process to fabricate 3C-SiC diaphragms.

test structures to determine the biaxial modulus and residual stress by investigating the load-deflection behavior of the diaphragms. This load-deflection technique uses an interferometer to measure the center deflection of a diaphragm experiencing an applied pressure. Deflection versus applied pressure data is acquired and fit to a model that contains terms dependent on the biaxial modulus and residual stress.[42]

The load-deflection technique has been used on both 3C-SiC and poly-SiC diaphragms. For diaphragms fabricated from 3C-SiC films grown by APCVD on small Si substrates, an average biaxial modulus of 441 GPa and average residual stress of 221 MPa were reported.[43] No dependence on film thickness was found for the biaxial modulus; whereas, residual stress decreased with increasing thickness. Biaxial modulus and residual stress for both 3C-SiC and poly-SiC films grown by LPCVD have also been studied.[44] It was reported that for 3C-SiC films of thicknesses up to 1.3 μm, the biaxial modulus was about 450 GPa, while the residual stress was about 150 MPa. For poly-SiC films of thicknesses up to 5.0 μm, the biaxial modulus was nearly that of the 3C-SiC films, averaging 465 GPa, while residual stress could be adjusted from 0 to 250 MPa by changing the deposition parameters. Another study investigated the change in biaxial modulus as a function of dopant gas concentration for LPCVD poly-SiC. This study found that for increasing boron concentrations (for B/Si ratios up to 0.02), the biaxial modulus peaked at 600 GPa, as compared to 480 GPa for undoped films.[45] Residual stress values for these films were not reported.

Other bulk micromachined structures have been used to determine the mechanical properties of 3C-SiC films. A vibrating membrane technique was used to determine the residual stress in 3C-SiC films grown on Si substrates.[46] It was reported that the residual stresses were highest in p-type films as compared with n-type and undoped films. It was also reported that the internal stresses in doped and undoped films decreased with increasing temperature up to 600°C. By extrapolating the linear portion of the stress versus temperature data to high temperatures, it was found that zero stress occurred between 1250°C and 1350°C, which corresponded to the growth temperature of the films. Thus, it was concluded that the films were grown under stress-free conditions, and therefore the internal stress measured at room temperature was due to the thermal mismatch between the 3C-SiC films and the Si substrates. In a different study, the free-standing microcantilever beams shown in Fig. 4.2 were used to investigate the bending moment caused by the residual stress gradient in 3C-SiC films.[47] The average bending moment was about

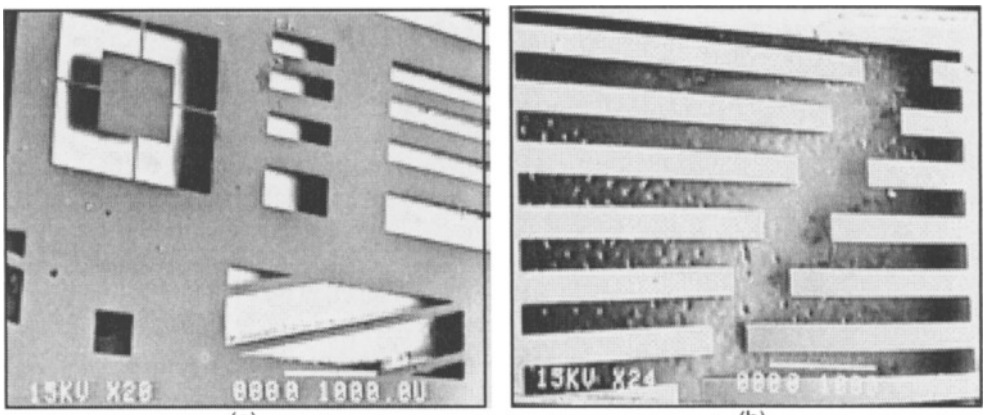

Fig. 4.2. (a) SEM micrographs of bulk-micromachined SiC suspensions[43] and (b) cantilever beams.

3.4×10^8 Nm. Using a vibrating cantilever technique, the Young's modulus (which is closely related to the biaxial modulus) for 3C-SiC films was measured to be about 694 GPa for undoped 3C-SiC and 474 GPa for p-type 3C-SiC.[48]

The spatial variation of the biaxial modulus and of the residual stress of 3C-SiC films deposited by APCVD on large-area substrates has been studied.[41] The load-deflection technique was applied to 12 diaphragms taken from well-distributed locations across each wafer. It was reported that under all deposition conditions, the spatial variation of the biaxial modulus and of the residual stress was lowest within the center 3-in. diameter of a 4-in.-diam wafer. In the same study, the variation in the biaxial modulus and in the residual stress as a function of precursor gas flow rates and deposition temperatures was investigated. In general, at a fixed deposition temperature (1280°C), high precursor gas flow rates produced 3C-SiC films with lower average residual stresses (112 MPa) and higher biaxial moduli (348 GPa) than low flow rates (340 MPa, 294 GPa). At a lower deposition temperature (1160°C), the films changed from single to polycrystalline at both high and low flow rates. However, the residual stress increased significantly (from 112 to 311 MPa) for high flow rates, while only modestly (from 340 to 360 MPa) for low flow rates.

The variability of the mechanical properties in APCVD 3C-SiC films as a function of susceptor age and susceptor supplier has also been studied.[49] Susceptor age is defined by the total number of deposition hours a susceptor has been used for SiC growth. Early reports suggested that material deposited on the surface of susceptors during SiC growth may contribute to the deteriorating electrical and morphological properties of SiC films.[12] To study the influence of susceptor age on the mechanical properties, 3C-SiC films were grown under identical conditions 50 runs apart, which was equivalent to about 100 deposition hours. During this span, considerable changes were observed on the susceptor, namely, dark gray deposits along the upstream surfaces. Similar observations have been reported for films grown using small susceptors.[12] In terms of biaxial modulus and residual stress, no significant changes between the samples were noticed. Films grown using susceptors from two different manufacturers were also studied. The susceptors were "seasoned" by using them for 25 depositions prior to growing films for study. As in the susceptor age study, no significant differences were found between the samples. In terms of the mechanical properties of SiC films, this study shows that susceptors can be used for many depositions (>100 deposition hours), and that the performance of a susceptor is not dependent on the supplier.

4.5.2 Surface Micromachining

The first reported SiC surface micromachining process was developed for poly-SiC films deposited on polysilicon sacrificial layers.[50] A single-mask lateral resonant structure was chosen as the demonstration vehicle. A schematic cross section of the fabrication process and a scanning electron microscopy (SEM) micrograph of the device are shown in Figs. 4.3(a) and 4.3(b). The substrate was prepared by first growing a 1-μm-thick thermal oxide on a silicon wafer. The thermally grown SiO_2 layer provided electrical isolation and protected the Si substrate during release. A 2-μm-thick polysilicon film was then deposited on the oxidized Si substrate. Poly-SiC was deposited on the polysilicon using the three-step SiC growth process (in-situ clean, carbonization, film growth) detailed earlier in this chapter. RIE was used in conjunction with photolithography to pattern the poly-SiC film into the desired shape. The free-standing sections of the resonator were released by using a timed etch in KOH, which does not etch the poly-SiC or the thermal oxide. Supercritical drying was used to minimize stiction problems associated with the release. To operate the devices, an actuation voltage ranging between 30 and 175 V was required. These devices had a resonant frequency of 20 kHz.

Although polysilicon is an adequate sacrificial layer material for SiC surface micromachining, SiO_2 is preferred, since it can be used as both the electrical isolation layer and sacrificial layer. A

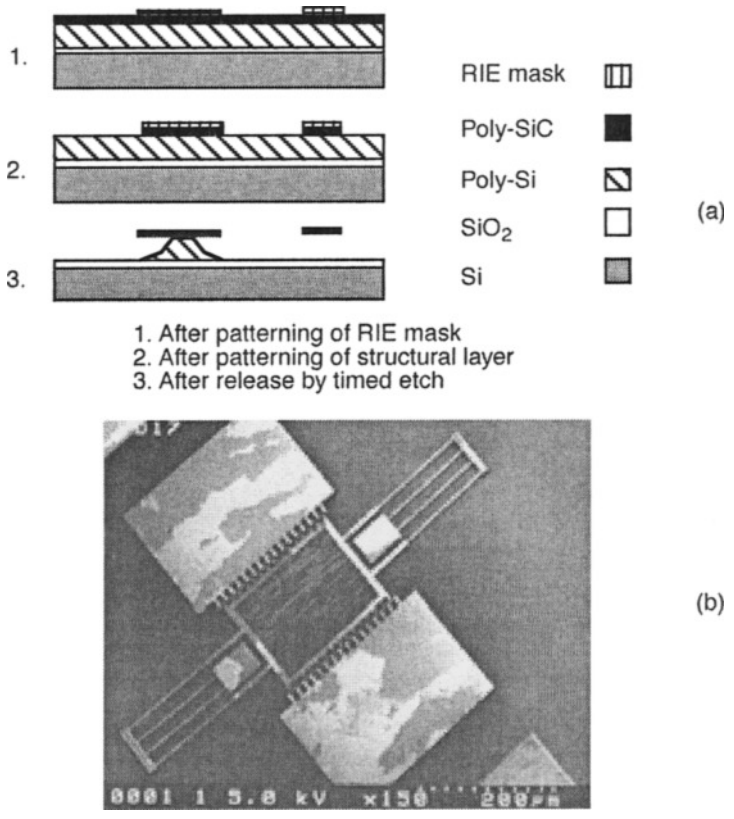

Fig. 4.3. (a) Schematic diagram of a SiC surface micromachining process using a polysilicon sacrificial layer. (b) SEM micrograph of a SiC surface micromachining lateral resonant structure fabricated using a polysilicon sacrificial layer.[50]

SiC surface micromachining process that uses a poly-SiC film deposited by APCVD on a SiO_2 sacrificial layer has been developed.[27] A schematic cross section and SEM micrograph of a lateral resonant structure are shown in Figs. 4.4(a) and 4. 4(b). These structures were fabricated from 2-μm-thick poly-SiC films grown on 3.5-μm-thick SiO_2 sacrificial layers on Si substrates. The poly-SiC films were photolithographically patterned using RIE to form the resonator structure. The devices were released by a timed etch in 49% HF solution, which etched the underlying SiO_2 to form the free-standing poly-SiC structures. The devices resonated at frequencies between 18 and 50 kHz using actuation voltages of about 50V.

To confirm the commonly held belief that SiC is a better mechanical material than Si at high temperatures, the resonant frequency response of poly-SiC and polysilicon lateral resonant structures was compared for devices heated to 900°C.[51] All devices used in this study were fabricated from 2-μm-thick films deposited on SiO_2 sacrificial layers using the same photolithographic mask and surface micromachining process. Testing was performed in an argon-filled chamber that was equipped with a heated sample stage capable of reaching temperatures above 1000°C. Figure 4.5 shows the behavior of the resonant frequency as a function of temperature for polysilicon [Fig. 4.5(a)] and poly-SiC [Fig. 4.5(b)] lateral resonant devices. For the polysilicon devices, the resonant frequency began to decrease at 350°C. The average rate of reduction in resonant frequency for the polysilicon devices between room temperature and 900°C was 1.11 Hz/°C. For temperatures above 350°C, the rate of reduction increased to 1.92 Hz/°C. For the poly-SiC devices, no detectable change in the resonant frequency was observed for temperatures below

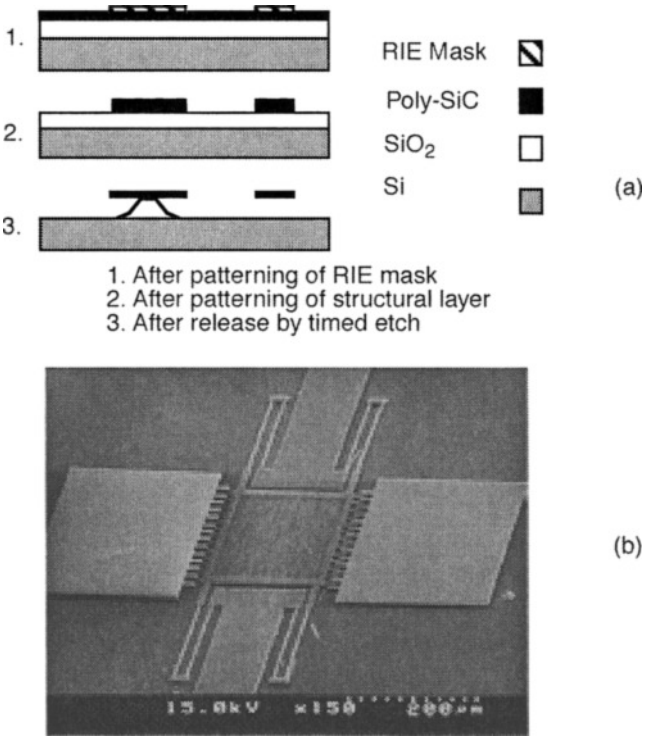

Fig. 4.4. (a) Schematic diagram of a SiC surface micromachining process using a SiO_2 sacrificial layer. (b) SEM micrograph of a SiC surface micromachining process using a SiO_2 sacrificial layer.[27]

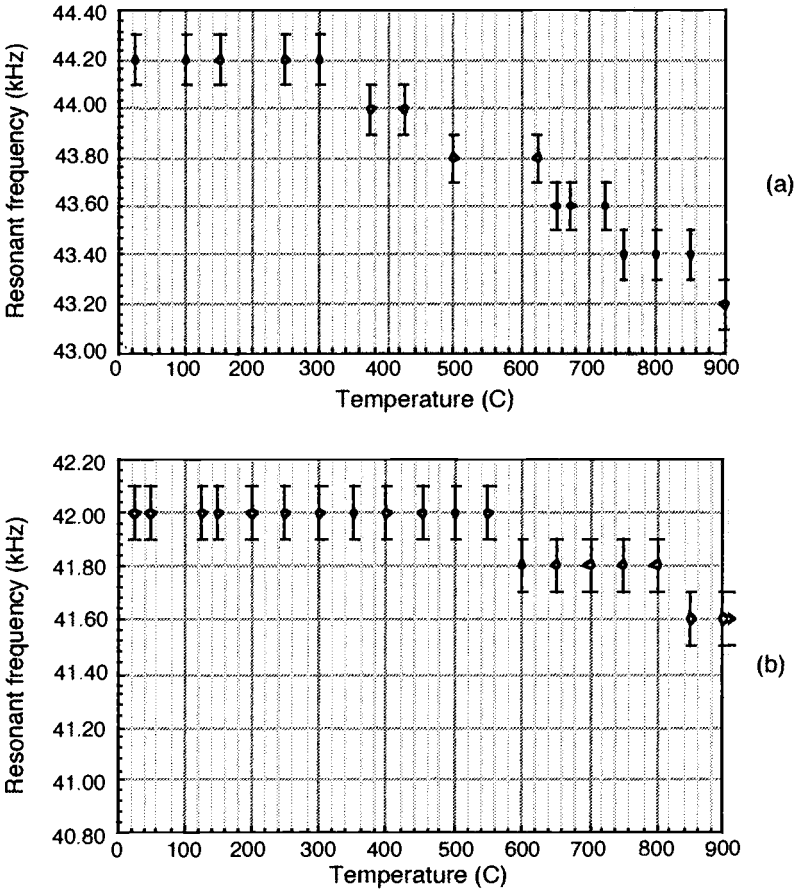

Fig. 4.5. Resonant frequency vs temperature data for lateral resonant devices (a) polysilicon and (b) poly-SiC.[51]

500°C. The average reduction in resonant frequency for the poly-SiC devices was 0.44 Hz/°C over the entire temperature range and 1.14 Hz/°C for temperatures above 500°C.

The resonant frequency of a lateral resonant structure is a function of device geometry and material properties and is described by the following equation:

$$f_r = \sqrt{\frac{hEw^3}{2\pi^2 m l^3}} \tag{4.1}$$

where h is thickness of the beams, E is the Young's modulus, w is the width of the beam, m is the mass of the device, and l is the length of the beam. If the thermal expansion properties of the device are taken into account, it can be shown that the thermal expansion of l and w will cancel out, and that the thermal expansion of h is very small and should cause an increase in the resonant frequency of the device. However, the resonant frequencies of both the poly-SiC and the polysilicon devices are reduced, implying that the Young's modulus for both materials is reduced at elevated temperatures. Poly-SiC, which exhibits a smaller variation in Young's modulus with increasing temperature, is superior to polysilicon as a structural material for high-temperature MEMS applications.

4.6 SiC-on-Insulator Technologies

Unlike poly-SiC, single crystal SiC cannot be grown directly on SiO_2 or on any other suitable nonconducting sacrificial material. Therefore, surface micromachining and electrical isolation of 3C-SiC structures and devices are very difficult. Because nitrogen is a shallow n-type donor in SiC and is easily incorporated during deposition and crystal growth processes, deposition of insulating SiC films is also very difficult. The need for electrically isolated single crystal SiC films has motivated researchers to borrow from silicon-on-insulator (SOI) fabrication techniques in order to produce SiC-on-insulator substrates. The three SiC-on-insulator fabrication processes that have been reported in the literature are: (1) growth of 3C-SiC on SOI substrates;[52–54] (2) the Smart-Cut™ process;[55] and (3) wafer bonding.[56]

The first process to fabricate electrically isolated 3C-SiC films used SOI wafers as substrates for epitaxial growth of 3C-SiC. The SOI wafers were produced either by ion implantation of O_2 into the subsurface region of an Si wafer (separation by implanted oxygen [SIMOX]), or by bonding two thermally oxidized Si wafers and removing all but a very thin layer of one of the wafers. The processing details for each of these techniques can be found elsewhere.[52–54] To create a SiC-on-insulator substrate from a SOI wafer, the thin Si layer atop the buried oxide must be fully converted to 3C-SiC; otherwise, a 3C-SiC-on-Si-on-SiO_2 structure is created. The conversion process occurs during the carbonization step, which limits the thickness of the Si layer to about 200 nm. It has been observed that during the carbonization process, out-diffusion of oxygen from the buried SiO_2 layer occurs, which creates sealed cavities at the 3C-SiC/SiO_2 interface.[53,54] These sealed cavities may adversely affect the electrical and mechanical properties of the structure. SIMOX substrates have limited high-temperature applications, because the thickness of the implanted oxide layer is limited to a few thousand angstroms, and the quality of the implanted oxide is poor when compared with thermal oxides.

The second SiC-on-insulator fabrication process, known as the Smart-Cut™ process, was first developed to produce SOI structures for silicon-based microelectronics.[55] The process combines ion implantation with wafer bonding to create a SOI substrate. Two Si wafers, hereafter called the handling wafer and the implant wafer, are thermally oxidized to form a thick (~1 μm) SiO_2 film on each wafer. The implant wafer then undergoes hydrogen ion implantation, which deposits hydrogen below the thermal oxide and below a thin layer of Si. After implantation, the SiO_2 surfaces of the two wafers are fusion bonded at high temperature. During this step, the implanted hydrogen condenses into a thin, well-defined region of voids. This region forms a seam that is used to remove the implant wafer from the bonded pair, thus transferring the thin Si layer to the handling wafer and creating an SOI substrate. The high-temperature bonding step also serves to anneal any ion-induced lattice damage in the thin Si layer. After bonding, the Si surface is polished and readied for processing.

By using 6H-SiC wafers as the implant wafers, the Smart-Cut™ process has been adapted to fabricate 6H-SiC-on-insulator substrates.[57] The 6H-SiC implant wafers have been successfully bonded to 6H-SiC, poly-SiC, and Si-handling wafers. These substrates may not be suitable for MEMS, since the overall area of a 6H-SiC-on-insulator substrate is limited by the size of the 6H-SiC implant wafer, which is currently only 2 in. in diameter. An additional concern is that implantation damage in the 6H-SiC layer is not annealed during the bonding step.[58] Annealing these defects may require temperatures that may damage the underlying SiO_2 layer.

The third SiC-on-insulator fabrication process uses wafer bonding to create SiC-on-insulator structures. A schematic of the process is shown in Fig. 4.6. The first wafer bonding process used SiO_2-to-SiO_2 bonding to create 3C-SiC-on-SiO_2 structures.[56] The process begins with epitaxial growth of 3C-SiC on a Si transfer wafer. The handling wafer is prepared by thermally oxidizing

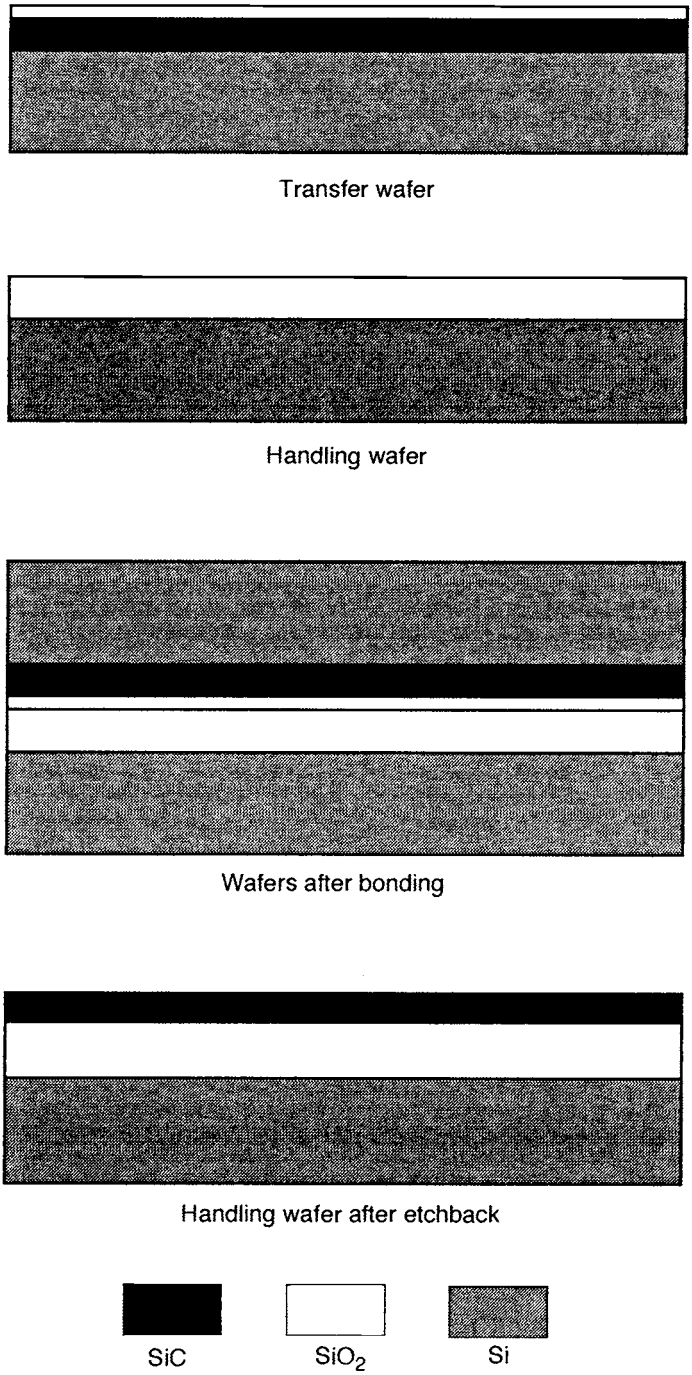

Fig. 4.6. .Schematic diagram of the 3C-SiC-on-SiO_2 wafer bonding process.

a Si wafer. A thermal oxide is also grown on the 3C-SiC film. The two SiO_2 surfaces are chemically treated and bonded. KOH etching is used to remove the SiC-coated transfer wafer, leaving a 3C-SiC-on-SiO_2 structure on the handling wafer. Unfortunately, only 30% of the SiC film area remains bonded after KOH etching, which is too low for batch processing.

A fourth improved wafer-bonding technique has been developed to produce 3C-SiC-on-SiO_2 structures on 4-in. Si wafers with areal transfer yields of up to 80%.[59] Unlike the third process mentioned above, the improved process utilizes a polysilicon-to-polysilicon bond to create the desired structure. A schematic of the process is shown in Fig. 4.7. The process begins with epitaxial growth of a 0.5-μm-thick 3C-SiC film on a 4-in. Si wafer, hereafter called the transfer wafer. The 3C-SiC film is chemically cleaned and thermally oxidized to produce a 0.3-μm-thick SiO_2 film on the 3C-SiC. A 0.5-μm-thick polysilicon film is then grown on the SiO_2 layer. The polysilicon is completely oxidized, which produces a total oxide thickness of 1.44 μm on the 3C-SiC film. Following the second thermal oxidation, a 2.0-μm-thick polysilicon film is deposited on the wafer and polished to a mirror finish by chemical-mechanical polishing. A 1.5-μm-thick thermal oxide is grown on a second wafer, hereafter called the handling wafer. A 2.0-μm-thick polysilicon film is deposited on top of the thermal oxide, and the polysilicon surface is polished to a mirror finish.

The polysilicon-to-polysilicon bonding process consists of three steps: (1) a prebond surface treatment, (2) room temperature bonding, and (3) high-temperature annealing. Step 1 is a standard wet chemical cleaning of the polished polysilicon surfaces. Step 2 places the polysilicon surfaces firmly together and uses van der Waals attraction to keep the surfaces in contact. Step 3 is an anneal at 1100°C in nitrogen for at least 5 h.

Following the anneal, the bonded pair is submerged in EDP, which removes the transfer wafer, leaving a 3C-SiC-on-SiO_2 structure atop the handling wafer. A SEM micrograph of the structure is shown in Fig. 4.8. The 3C-SiC film is too thin for most MEMS applications, so a thick (<1.0 μm) 3C-SiC film is homoepitaxially grown on the 3C-SiC-on-SiO_2 substrate. The substrate is prepared for homoepitaxial growth by a four-step process: (1) mechanical polishing, (2) thermal oxidation, (3) chemical etching, and (4) in-situ high-temperature hydrogen etching. Recall from previous discussions that the region of highest defect density in 3C-SiC films grown on Si substrates is near the SiC/Si interface. By transferring the heteroepitaxial film from the transfer wafer to the handling wafer, the bonding process brings the region of highest defect density to the surface of the bonded structure. Mechanical polishing with a SiC-based slurry is used to remove this region. Any defects created during the polishing step are removed by the thermal oxidation and chemical etching steps. Any residue on the 3C-SiC surface is removed immediately before homoepitaxial growth by the in-situ hydrogen etch, which is performed at 1000°C.

Figure 4.9 shows a TEM micrograph of the homoepitaxial 3C-SiC film grown on the 3C-SiC-on-SiO_2 structure. The TEM shows a clear reduction of crystalline defects in the homoepitaxial film, as compared with the underlying 3C-SiC, which was grown by the conventional 3C-SiC-on-Si heteroepitaxial process. The TEM observations were confirmed by rocking curve XRD. Although the physical mechanism responsible for the reduction of defects has not yet been identified, it is believed that the surface treatment prior to homoepitaxial growth plays a key role.

For the first time, large-area 3C-SiC can be produced atop insulating sacrificial substrates, making electrically isolated 3C-SiC surface-micromachined devices possible. The reduced defect density will improve the performance of both mechanical and electronic structures in 3C-SiC-based MEMS devices. The biggest impact, however, may be in the high-temperature and high-power microelectronics field, where low defect-density SiC films on large-area substrates are required. This technology may rekindle interest in 3C-SiC as a high-temperature semiconductor for microelectronics.

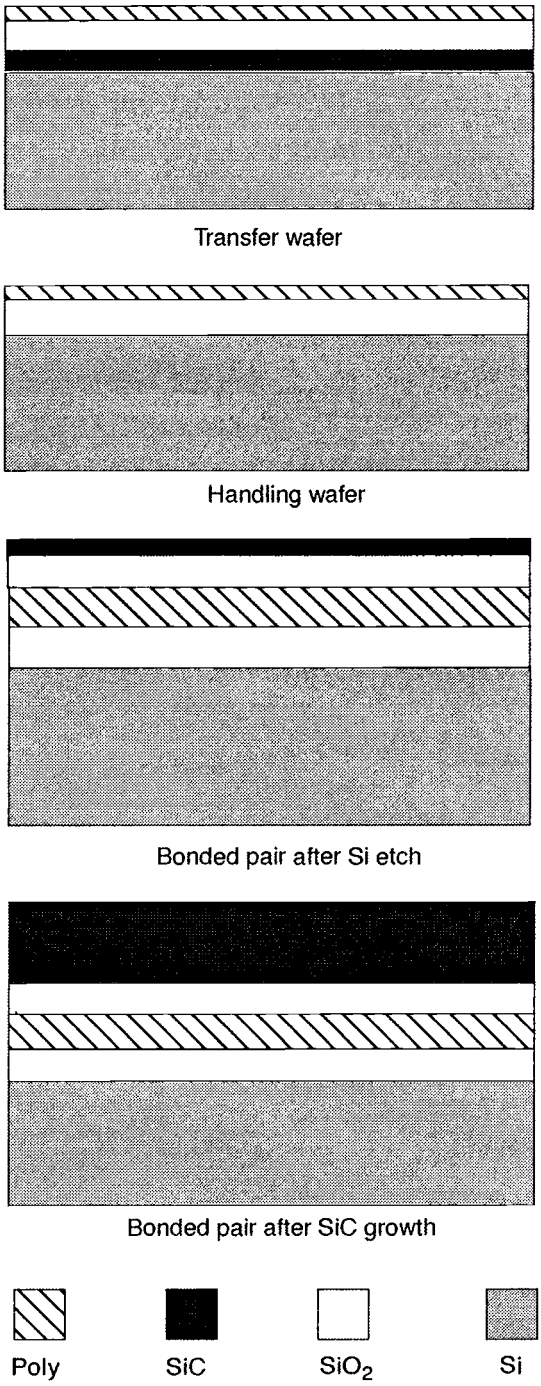

Fig. 4.7. Schematic diagram of the improved 3C-SiC-on-insulator fabrication process.

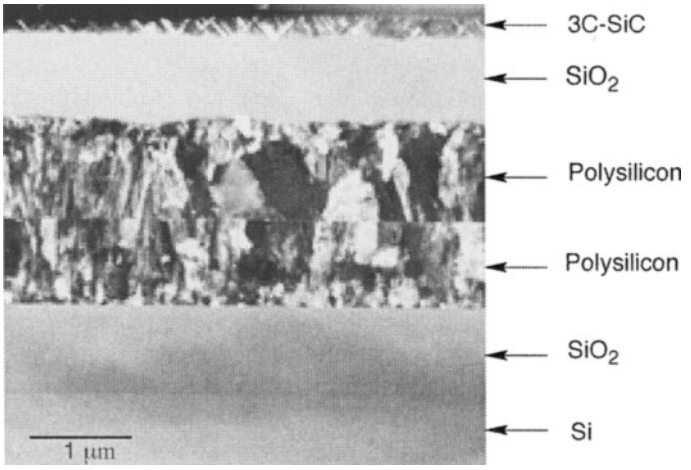

Fig. 4.8. TEM micrograph of a 3C-SiC-on-insulator structure, highlighting the polysilicon-to-polysilicon bonding interface.[59]

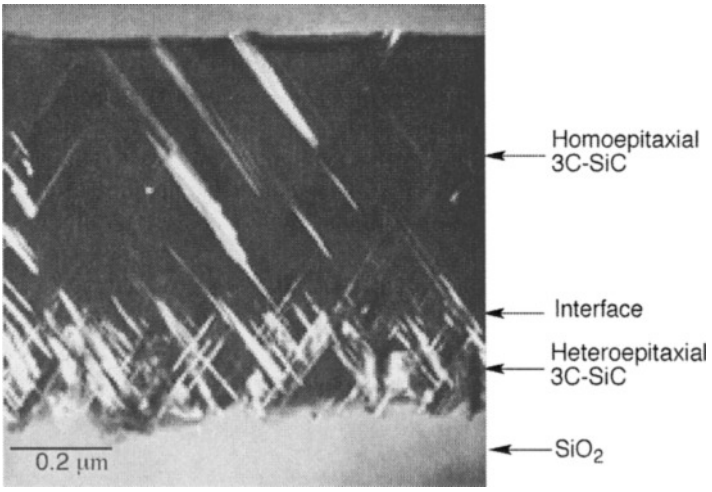

Fig. 4.9. TEM micrograph of a homoepitaxial 3C-SiC film grown on a 3C-SiC-on-insulator substrate, showing the decreased defect density in the homoepitaxial film.[59]

4.7 SiC Devices and Applications

4.7.1 Introduction

SiC research has concentrated on understanding the material properties and processing techniques required to use SiC as a high-temperature material for electronics. Only recently have the processing techniques become available to fabricate basic SiC-MEMS devices. This section will present descriptions of a representative collection of devices that use SiC as the key material for electronic and mechanical components. The devices have at least one common characteristic, high-temperature functionality, which makes them well suited for aerospace applications.

One of the principal focus areas for SiC-MEMS has been high-temperature SiC sensor systems for gas turbine engines. To improve the efficiency, power-to-weight ratios, emissions, cost, and

safety of gas turbine engines, new generation designs will require improved measurement, control, and sensor systems. These systems will often be located in or near the hot-gas flow path, which reaches temperatures above 350°C. Sensors are needed to measure combustor temperature, rotor and stator temperatures, internal cooling temperatures, cooling flow and temperature, pressure, hot gas path leakage, and coolant leakage. Sensors are also needed to control the engine near its combustion limit in order to maximize fuel combustion and minimize NO_x emissions.

Increasing the efficiency of the combustion process, through conversion of electronic control and sensor systems from Si- to SiC-based devices, will result in increased fuel economy and reduced emissions. In addition, the overall weight of an aircraft will be reduced by the elimination of the packaging, wiring, and connectors necessary to link sensor systems with control electronics. This weight reduction will directly translate to increased range and lower fuel costs.

SiC-based MEMS devices will also benefit manned and unmanned spacecraft. Currently, unmanned spacecraft require thermal radiators to dissipate heat generated by onboard Si-based electronics. Implementation of SiC-based electronic systems that can operate at temperatures above 400°C will eliminate the need for thermal radiators, thus reducing the overall weight of the spacecraft. Additionally, SiC electronics and sensors, being much less susceptible to radiation damage than their Si counterparts, will not require as much radiation shielding, thus reducing spacecraft weight even further. Reduced spacecraft weight and increased operating temperature and radiation resistance of onboard electronics and sensor systems will dramatically increase the functionality of unmanned spacecraft. Exploratory spacecraft will be able to more aggressively probe harsh planetary environments. Communication satellites will have extended operating lifetimes and will be able to carry larger numbers of sensitive onboard electronic systems.

In terms of propulsion systems, many high-temperature sensor systems will find applications in rocket motors. High-temperature sensors to monitor combustion temperature, pressure, and by-products are needed. Gas sensors for hydrogen and HCl are required for chemical detection around the launch pad and as part of in-flight safety systems. All of these systems can be fabricated from SiC.

The remainder of this section presents examples of SiC-based sensors for high-temperature MEMS applications. These sensors constitute the basic units of MEMS for the aeronautic and space applications mentioned previously. These sensor prototypes have demonstrated high-temperature functionality but require the development of high-temperature wire bonding and packaging technologies, and integration with on-chip SiC electronics before deployment in aerospace systems can occur.

4.7.2 Temperature Sensors

Some of the first SiC-based sensors were fabricated from poly-SiC because of the many methods available for deposition and the ability to deposit poly-SiC on many different substrates. One of the first sensors was a SiC thin-film thermistor.[60] The sensor was fabricated from radio frequency (RF) sputter-deposited SiC, using an Ar sputtered SiC target and a deposition pressure of 20 mtorr. The SiC film was deposited on an alumina substrate that was maintained at a deposition temperature of 650°C. Au-Pt comb-shaped thick films were used as electrodes. Various packages for the thermistor were developed and tested at temperatures between 0°C and 500°C. It was reported that the thermistor constant (B) increased linearly with temperature over the entire temperature range. Also, when compared with conventional metal-oxide thermistors, the temperature coefficient of resistance for the SiC thermistors decreased more slowly with increasing temperature. Additionally, the sensor exhibited good thermal stability and a rapid thermal response. A resistance change of only 5% was observed for a continuous 1000 h test at 500°C.

The fabrication of a SiC-based resistive temperature sensor has also been reported.[61] SiC films for this sensor were prepared by plasma-assisted chemical vapor deposition (PACVD), using dichlorosilane and methane as the Si and C source gases. Stoichiometric poly-SiC films were obtained with a dichlorosilane flow rate of 15 sccm, a methane flow rate of 5 to10 sccm, RF power of 70 W, and a substrate temperature of 750°C. The poly-SiC films were deposited on thermally oxidized Si substrates and patterned into resistors by RIE. To reduce thermal conduction to the substrate, the resistors were made into cantilever structures by bulk micromachining the Si substrate in KOH. The contact pads remained anchored to the substrate. The resistors were tested at temperatures between 0°C and 300°C, and exhibited a temperature coefficient of resistance of −1800 ppm/°C. The sensor was placed into a nitrogen flow stream to evaluate its performance as a gas mass flow sensor. The output characteristics of the SiC sensor showed a square-root dependence, which is characteristic of micromachined flow sensors.[62] The output sensitivity of the SiC mass flow sensor was 0.05 mV/sccm.

4.7.3 Gas Sensors

Interest in high-temperature semiconductors for solid-state gas and chemical sensors stems from the need for closed-loop control of the combustion process in gasoline and gas turbine engines. This control is needed to increase fuel and combustion efficiency, thereby decreasing emissions of incompletely combusted hydrocarbons, nitrous oxides (NO_x), and CO_2. Currently, the dominant polytype used for SiC-based gas sensors is 6H-SiC, because 6H-SiC has the highest crystal quality of all the commercially available polytypes. The 6H-SiC gas sensors are based on simple Schottky diode and metal-oxide-semiconductor (MOS) structures.

A common method for fabricating SiC-based gas sensors uses 6H-SiC MOS capacitors.[63] Called MOSiC (metal-oxide-SiC) structures, these sensors use catalytic metals such as Pt and Pd as the gate metals. The sensors work on the principle that hydrogen atoms or hydrogen-containing radicals diffusing through the gate will collect at the metal-oxide interface and form a dipole layer that lowers the flat band voltage of the MOS capacitor. Hydrogen sensors have been fabricated using Si MOS structures, but the operating temperature is limited to below 250°C. However, many hydrocarbons dissociate at temperatures between 350°C and 500°C, making SiC the better material for solid-state MOS hydrocarbon gas sensors.

The MOSiC gas sensor is made using a 6H-SiC substrate, on which a 40-nm-thick SiO_2 layer is thermally grown.[64] Approximately 50 nm of Pt is then deposited by either e-beam evaporation or magnetron sputtering on the SiO_2 surface, and patterned to form the MOSiC structure. This sensor has been tested at temperatures as high as 800°C without failing. At 450°C, the sensor was able to detect the presence of saturated hydrocarbons such as methane, propane, ethane, and butane at concentrations below 0.6 vol%. Moreover, the sensor can be used at elevated temperatures in vacuum or in air. The response of the sensor increases with an increasing number of carbon atoms in the detected molecule. With an operating temperature well above 500°C, this sensor is well suited for deployment in exhaust streams near the combustion chamber.

A second type of SiC gas sensor is based on the 4H-SiC Schottky diode.[65] The sensor is constructed from 4- to 5-μm-thick 4H-SiC films epitaxially grown on 4H-SiC substrates. Approximately 400 Å of Pd is sputter deposited and patterned to form circular contacts to the 4H-SiC. The sensor has been tested over a temperature range of 0°C to 400°C in a hydrocarbon environment and exhibits a sensitivity of 300 ppm to hydrogen and propylene.

A third type of SiC gas sensor uses porous SiC.[66] The sensor consists of a chromium (Cr) grid that is evaporated and patterned onto a layer of porous SiC. The porous layer is formed by PEC etching of a n-type 6H-SiC wafer. The thickness of the porous layer was not reported. A nickel

contact is deposited on the nonporous backside of the 6H-SiC wafer. A voltage is applied to the Cr grid, which sets up a voltage in the porous SiC region. Each hydrocarbon species has a characteristic dissociation voltage, so by varying the grid voltage, a specific hydrocarbon species can be forced to dissociate. The concentration of each species is determined by measuring the magnitude of current flow across the device for a given grid voltage. This sensor is an improvement over the previously mentioned sensors because it does not require high temperatures to operate, yet it can operate at high temperatures. Tests using methane and propane conducted at temperatures between 200°C and 500°C verified these capabilities.

4.7.4 Pressure Sensors

A 6H-SiC-based pressure sensor that exhibits stable operation at 500°C has recently been developed.[67] The sensor uses n-type 6H-SiC piezoresistors on a p-type 6H-SiC diaphragm. The diaphragm is fabricated using the PEC etching process of 6H-SiC described previously and detailed elsewhere.[38] During development of the etching process, a p-type etch stop for n-type etching was demonstrated. The fabrication process begins with epitaxial growth of a p-type 6H-SiC film on an n-type 6H-SiC wafer, followed by epitaxial growth of an n-type 6H-SiC film on the p-type epilayer. PEC is used to bulk-micromachine the n-type 6H-SiC wafer into 50-μm-thick diaphragms, and pattern the n-type 6H-SiC into piezoresistors. Multilayer Ti/TiN/Pt/Au metal contacts are used in conjunction with Au wire bonding to package the device. A full-scale output of 40.66 mV at 1000 psi and 25°C, decreasing to 20.33 mV at 500°C, was reported. The device has a gauge factor temperature coefficient of -0.19%/°C at 100°C and -0.11%/°C at 500°C. Despite the attractiveness of an "all-SiC" high-temperature pressure sensor, small 6H-SiC wafer diameters and nonstandardized fabrication processes currently limit the commercial application of this design.

A second pressure sensor design utilizes 3C-SiC films grown on SOI substrates combined with Si bulk micromachining to produce dielectrically isolated 3C-SiC piezoresistors on a thick Si membrane.[68] The piezoresistors are realized by conventional heteroepitaxial growth of 3C-SiC on the SOI substrates, followed by photolithography and reactive ion etching. The buried oxide in the SOI substrate prohibits leakage currents between the 3C-SiC piezoresistors and the Si substrate, a problem that is magnified at high temperatures. For each sensor, a circular Si diaphragm was micromachined to a thickness of 100 μm using RIE in a SF_6/O_2 plasma, and four 3C-SiC piezoresistors were patterned using SF_6/O_2 RIE. A thermally grown capping oxide over the piezoresistors was used for electrical isolation. Sputter-deposited TiWN alloy was used as high-temperature ohmic contacts. The sensor was tested in the temperature range between 25°C and 400°C, and at pressures up to 500 kPa. The sensor showed a linear output voltage over the applied pressure range and a sensitivity of –0.16%/°C at 400°C. Recently, a hermetic pressure sensor capsule for the SiC-based pressure sensor was constructed and tested.[2] This sensor design takes advantage of well-established Si micromachining techniques. However, the hybrid SiC/Si device may suffer from SiC/Si thermal mismatch effects, which may degrade long-term device performance and lifetime.

4.7.5 Protective Coatings

Micromachining is a technology that is not limited to the production of only microsensors and microactuators, but can be used to batch fabricate component structures for macroscale systems. A fine example is the development of micromachined silicon fuel atomizers as an alternative for conventional metal atomizers in gas turbine engines. A process to batch fabricate silicon atomizers from 4-in. Si wafers using deep reactive ion etching (DRIE) has been demonstrated.[69] A schematic and SEM micrograph of a Si-micromachined atomizer are shown in Figs. 4.10(a) and 4.10(b). Comparative tests of conventional metal and Si atomizers indicated that the Si atomizers

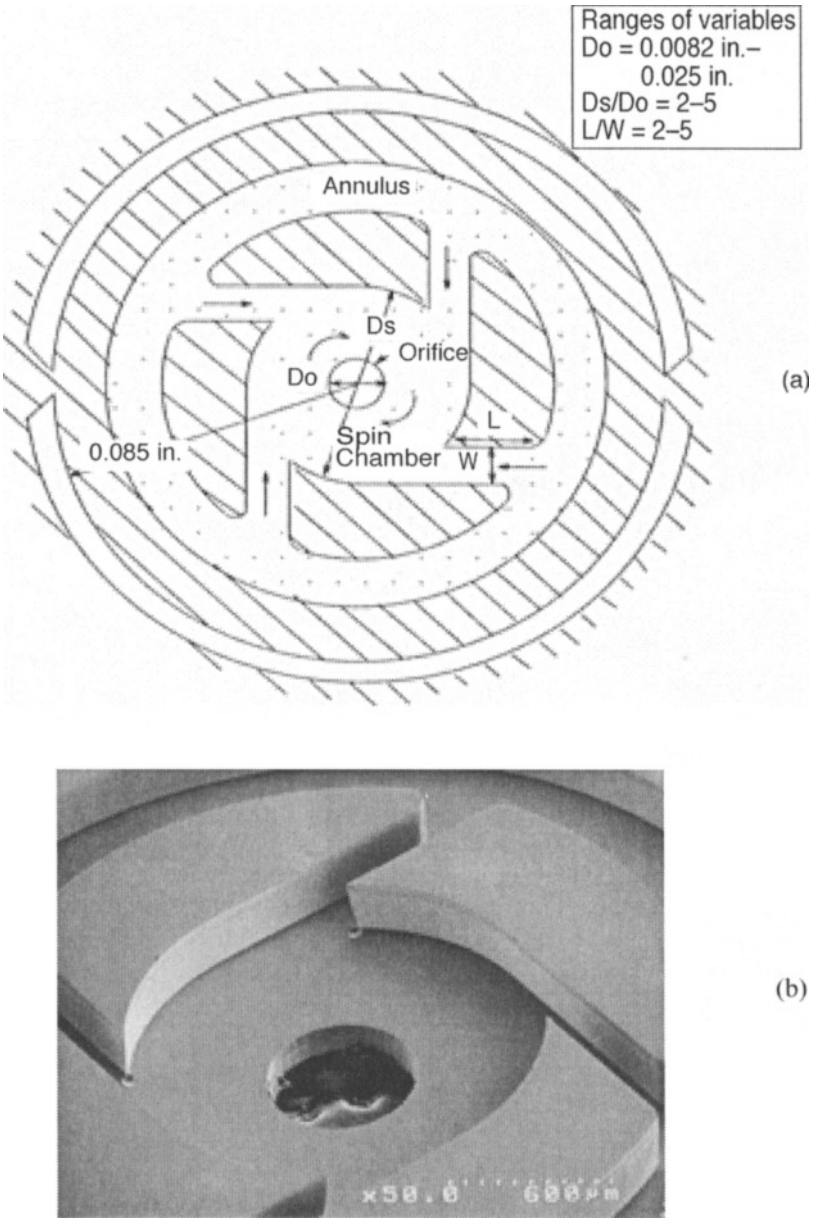

Fig. 4.10. (a) Schematic plan-view diagram of a fuel atomizer. (b) SEM micrograph of a silicon micromachined fuel atomizer.[69]

outperformed conventional atomizers, especially at low pressures. Unfortunately, the Si atomizers lacked the erosion resistance of conventional atomizers. A 3C-SiC coating was grown on the Si atomizers in hopes of increasing the erosion resistance of the structures.[70] Because the atomizers were fabricated from single crystalline Si wafers, the high-temperature deposition process with carbonization was used. This was the first attempt at growing 3C-SiC on high-aspect-ratio

Si topographies. Conformal coverage of the atomizer surfaces was achieved, with thicknesses ranging from 1.5 μm on the top surfaces to 0.5 μm on the swirl chamber floor.

The performance of the SiC-coated atomizers, in terms of flow rate, Sauder Mean Diameter (SMD), and spray angle, was compared with uncoated silicon atomizers. The test fluid was MIL-C-7024D Type II jet fuel stimulant. The flow rates for the coated atomizers were consistently 7%–11% higher than the uncoated atomizers. The SMDs were the same for both atomizer types. Higher spray angles at both low pressure (14 psi) and high pressure (100 psi) were also observed for the 3C-SiC coated atomizers. The spray angle is a rough gauge of atomizer efficiency, with wider spray angles indicating better performance.

To qualitatively determine the improvement of the erosion resistance of the SiC coated atomizers, a 30-h erosion test was performed. The test fluid consisted of jet fuel mixed with abrasives like iron oxide, quartz, and Arizona road dust. The test fluid was pressurized to 150 psi. SEM analysis of the region near the exit orifice was performed, since this region is subject to the highest erosive damage. The uncoated atomizers showed significant edge rounding near the exit orifice; whereas, the coated atomizers showed no evidence of edge rounding.

4.8 Conclusions

The field of SiC MEMS for high-temperature applications has advanced beyond material characterization and process development toward the fabrication of prototype devices that have been tested in harsh, high-temperature environments. Development of sensors and actuators will most certainly continue, and as early prototypes are successfully tested, more application areas and designs will be conceived. This will result in additional materials characterization and process development, as more sophisticated device structures are required.

Advances in two closely related areas will be required before SiC MEMS can make an impact in commercial and military applications: (1) reliable SiC electronics, and (2) viable high-temperature wire bonding and packaging technologies. Fortunately, research on SiC-based electronics for high-temperature applications has been and will continue to be a priority, and as larger area, defect-free 6H-SiC and 4H-SiC wafers become available, improvements in device performance will occur. Advances in wire bonding techniques and packaging technologies for high-temperature applications, which have been few to date, are expected to grow with advances in SiC electronics, sensor, and actuator technologies. By all indications, the future looks bright for SiC-based MEMS for applications in harsh environments.

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